

USB4 2.0 ENGINEERING CHANGE NOTICE FORM

Title: PCIe Segment in Downstream Entry Mapping Applied to: USB4 Specification Version 2.0

Brief description of the functional changes:

Exposing the PCIe Segment Mapping and making the 'Get PCIe Downstream Entry Mapping' Operation optional for Host Routers.

Benefits as a result of the changes:

Making the 'Get PCIe Downstream Entry Mapping' operation optional for Host Routers, and adding the Segment ID to the Completion. The current specification definition only exposes the Routing ID without the PCIe Segment, which is needed for some implementations to distinguish between several RCs.

Note: PCIe segment ID is of different length in various PCIe specifications (Firmware spec, Base Spec) so for 8b PCIe Segment the 8 least-significant bits are used while the most-significant bits are set to 0.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

NA

An analysis of the hardware implications:

NA

An analysis of the software implications:

NA

An analysis of the compliance testing implications:

Operation made optional. Dedicated test can be added for the new Capability fields.

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Actual Change

(a). Section 8.3.1.3 Router Discovery Operations

From Text:

8.3.1.3 Router Discovery Operations

Get PCIe Downstream Entry Mapping (Conditional)

A Connection Manager uses this Operation to retrieve information about the mapping of a PCIe downstream facing port. The mapping information is returned in an entry, where there is one entry per PCIe downstream facing port. Each execution of this Operation retrieves the entry for one PCIe downstream facing port. Entries are returned in increasing order of their Entry Index.

A Router shall support the Get PCIe Downstream Entry Mapping Router Operation if it supports PCIe Tunneling. This Router Operation is not applicable for a Router that does not support PCIe tunneling.

To Text:

8.3.1.3 Router Discovery Operations

Get PCIe Downstream Entry Mapping (Conditional)

A Connection Manager uses this Operation to retrieve information about the mapping of a PCIe downstream facing port. The mapping information is returned in an entry, where there is one entry per PCIe downstream facing port. Each execution of this Operation retrieves the entry for one PCIe downstream facing port. Entries are returned in increasing order of their Entry Index.

A **Device** Router shall support the Get PCIe Downstream Entry Mapping Router Operation if it supports PCIe Tunneling. **A Host Router may optionally support this Router Operation if it supports PCIe Tunneling.** This Router Operation is not applicable for a Router that does not support PCIe tunneling.

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(b). Section 8.3.1.3.1 Get PCIe Downstream Entry Mapping (Conditional)

From Text:

Table 8-48. Get PCIe Downstream Entry Mapping Completion Data

DW	Bit(s)	Field Name and Description
0	0	Native PCIe Link 0 – Entry is for a PCIe downstream facing port connected to a Downstream PCIe Adapter 1 – Entry is for a PCIe downstream facing port connected through a native PCIe link
	6:1	PCIe Adapter Number If <i>Native PCIe Link</i> is set to 0, this field shall indicate the Adapter Number of the Downstream PCIe Adapter. Otherwise it shall be set to 0.
	31:7	Reserved
1	15:0	Non-FPB Routing ID The Routing ID value assigned to this PCIe downstream facing port according to the non-FPB addressing scheme. A value of 0 indicates that the non-FPB addressing scheme is not used through this PCIe downstream facing port, unless both the Non-FPB Routing ID and FPB Routing ID fields to zero, which indicates that the non-FPB addressing scheme is used.
	31:16	FPB Routing ID The Routing ID value assigned to this PCIe downstream facing port according to the FPB addressing scheme. A value of 0 indicates that the FPB addressing scheme is not used through this PCIe downstream facing port.
2-15	31:0	Reserved

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To Text:

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0	0	Native PCIe Link 0 – Entry is for a PCIe downstream facing port connected to a Downstream PCIe Adapter 1 – Entry is for a PCIe downstream facing port connected through a native PCIe link
	6:1	PCIe Adapter Number If <i>Native PCIe Link</i> is set to 0, this field shall indicate the Adapter Number of the Downstream PCIe Adapter. Otherwise it shall be set to 0.
	14:7	Reserved
	15	PCIe Segment ID Valid When set – the PCIe Segment ID field is valid. When not set -the PCIe segment ID is not used or is set by implementation-specific means.
	23:16	PCIe Segment ID [7:0] The least significant byte of the Segment ID assigned to the PCIe downstream facing port. This field is valid in case the <i>PCIe Segment ID Valid</i> is set to 1. Otherwise this field shall be set to 0.
	31:24	PCIe Segment ID [15:8] This field contains the most significant byte of the Segment ID in case <i>PCIe Segment ID Valid</i> is set and the Segment ID size is 16-bits. Otherwise this field shall be set to 0.
1	15:0	Non-FPB Routing ID The Routing ID value assigned to this PCIe downstream facing port according to the non-FPB addressing scheme. A value of 0 indicates that the non-FPB addressing scheme is not used through this PCIe downstream facing port, unless both the Non-FPB Routing ID and FPB Routing ID fields to zero, which indicates that the non-FPB addressing scheme is used.
	31:16	FPB Routing ID The Routing ID value assigned to this PCIe downstream facing port according to the FPB addressing scheme. A value of 0 indicates that the FPB addressing scheme is not used through this PCIe downstream facing port.
2-15	31:0	Reserved